Title: RETURN PATH TRANSMITTER WITH EXTENDED DIGITAL PROCESSING CIRCUITRY
Inventors: Andrew R. Williams
Docket No.: 15436.253.78.1

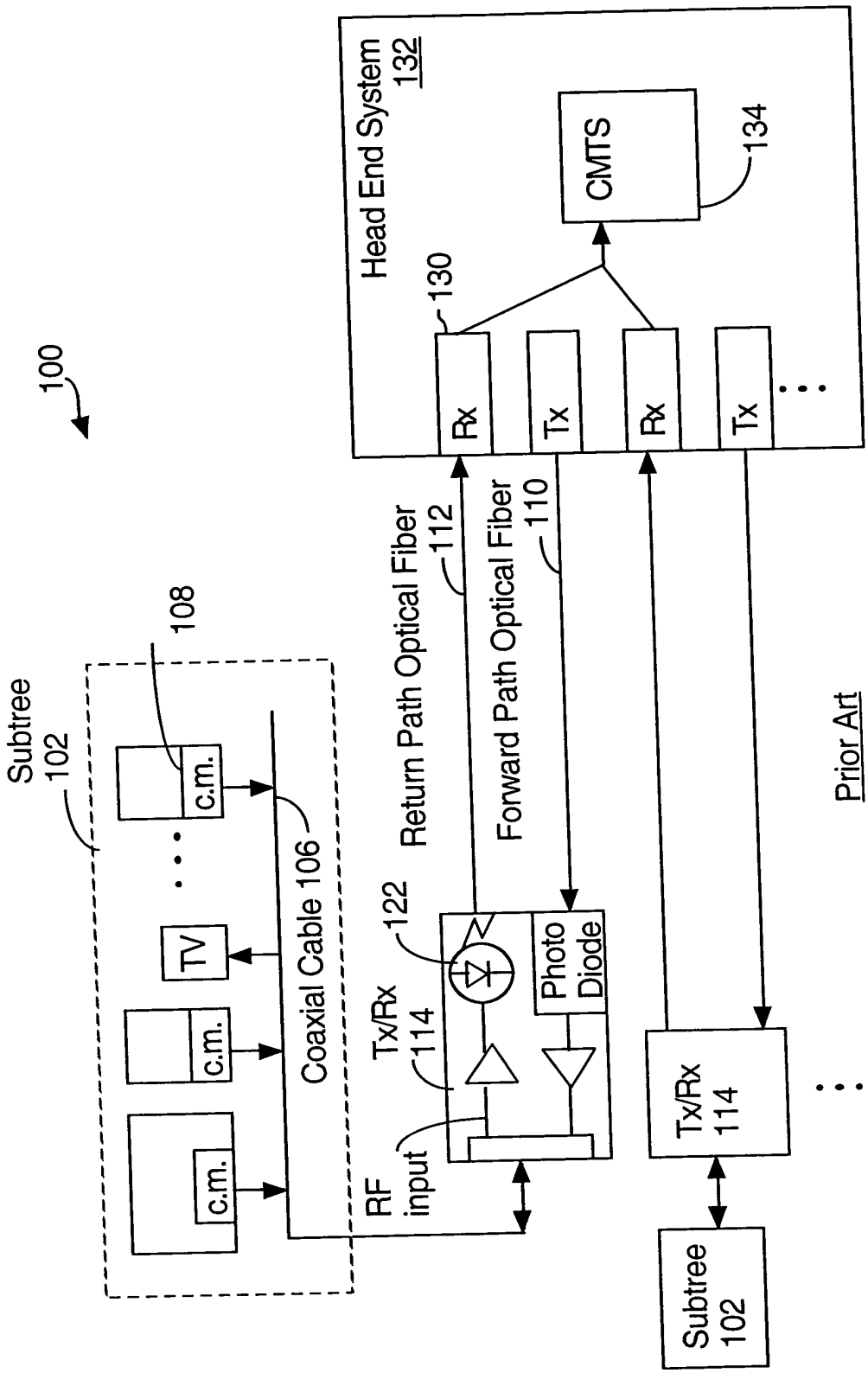


FIG. 1

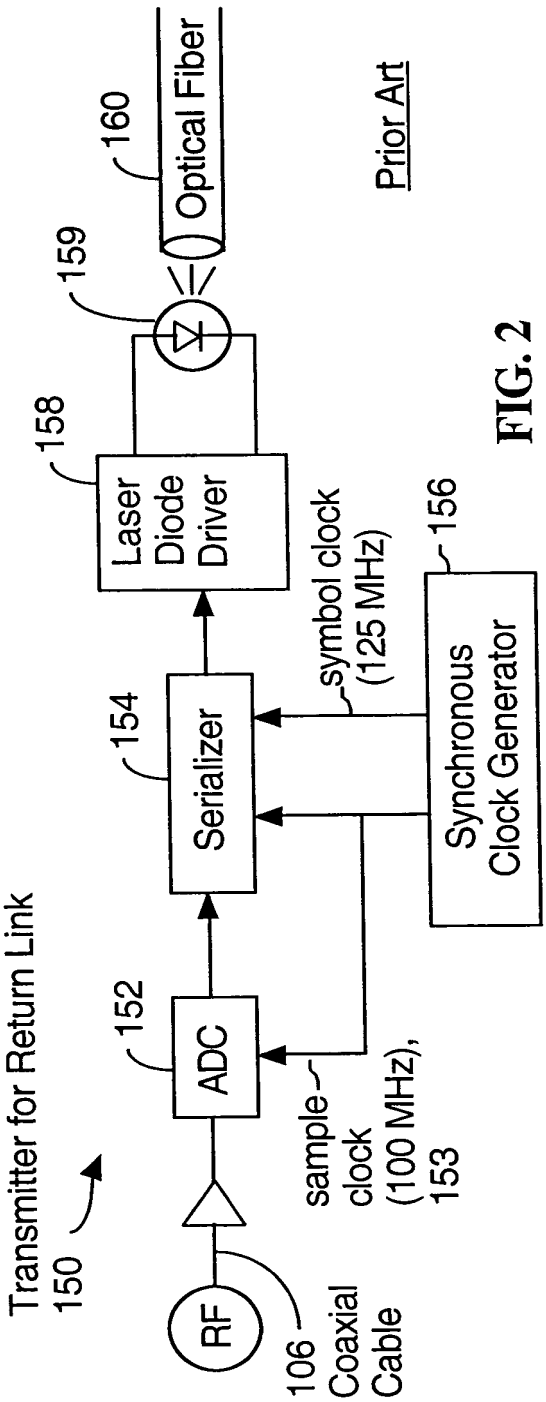

Transmitter for Return Link
150
RF
106
Coaxial
Cable
ADC
152
Serializer
154
Laser
Diode
Driver
158
Optical Fiber
160
159
sample
clock
(100 MHz),
153
symbol clock
(125 MHz)
Synchronous
Clock Generator
156
Prior Art

FIG. 2

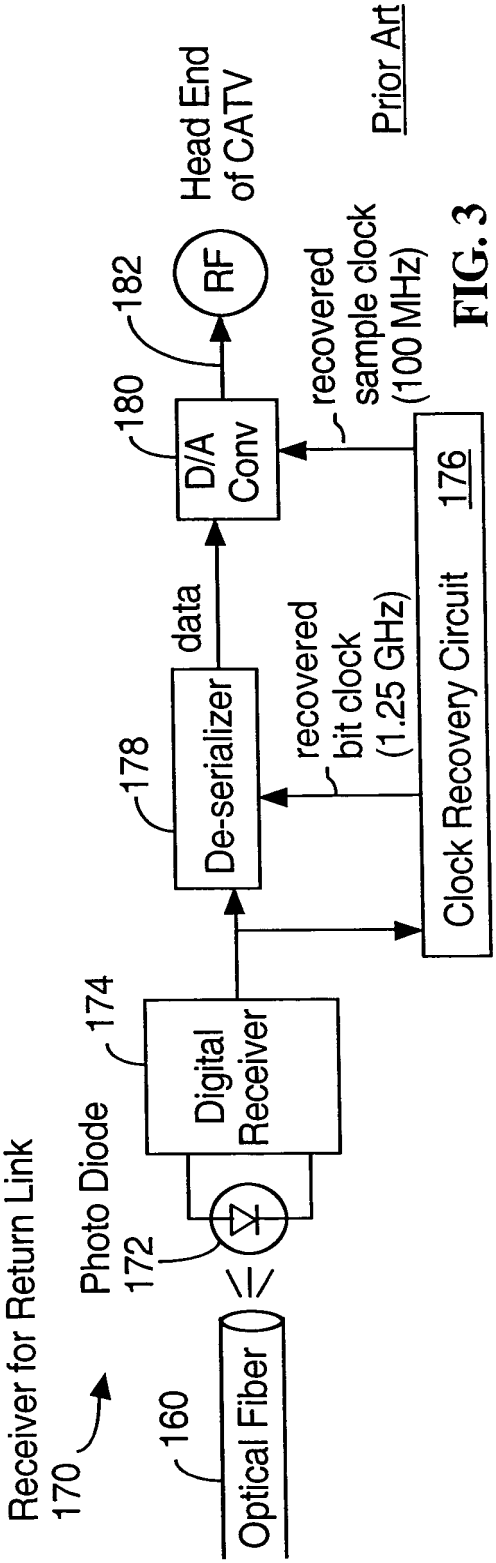

Receiver for Return Link
170
Optical Fiber
160
Photo Diode
172
Digital
Receiver
174
De-serializer
178
data
D/A
Conv
180
RF
182
Head End
of CATV
recovered
bit clock
(1.25 GHz)
recovered
sample clock
(100 MHz)
Clock Recovery Circuit
176
Prior Art

FIG. 3

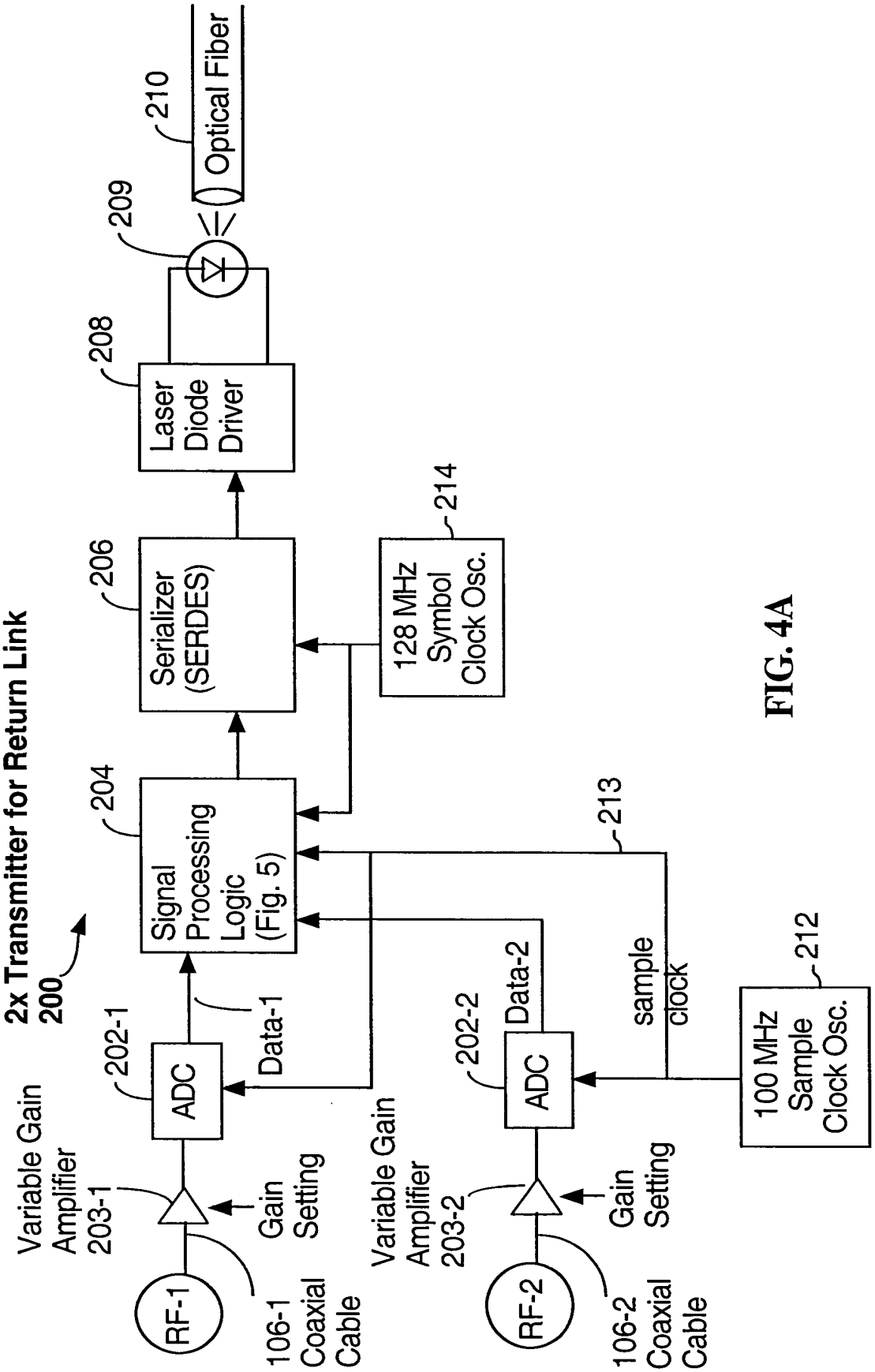

2x Transmitter for Return Link
200
RF-1
RF-2
106-1 Coaxial Cable
106-2 Coaxial Cable
Variable Gain Amplifier 203-1
Variable Gain Amplifier 203-2
Gain Setting
Gain Setting
202-1
202-2
ADC
ADC
Data-1
Data-2
204
Signal Processing Logic (Fig. 5)
206
Serializer (SERDES)
208
Laser Diode Driver
209
210
Optical Fiber
214
128 MHz Symbol Clock Osc.
213
sample clock
212
100 MHz Sample Clock Osc.

FIG. 4A

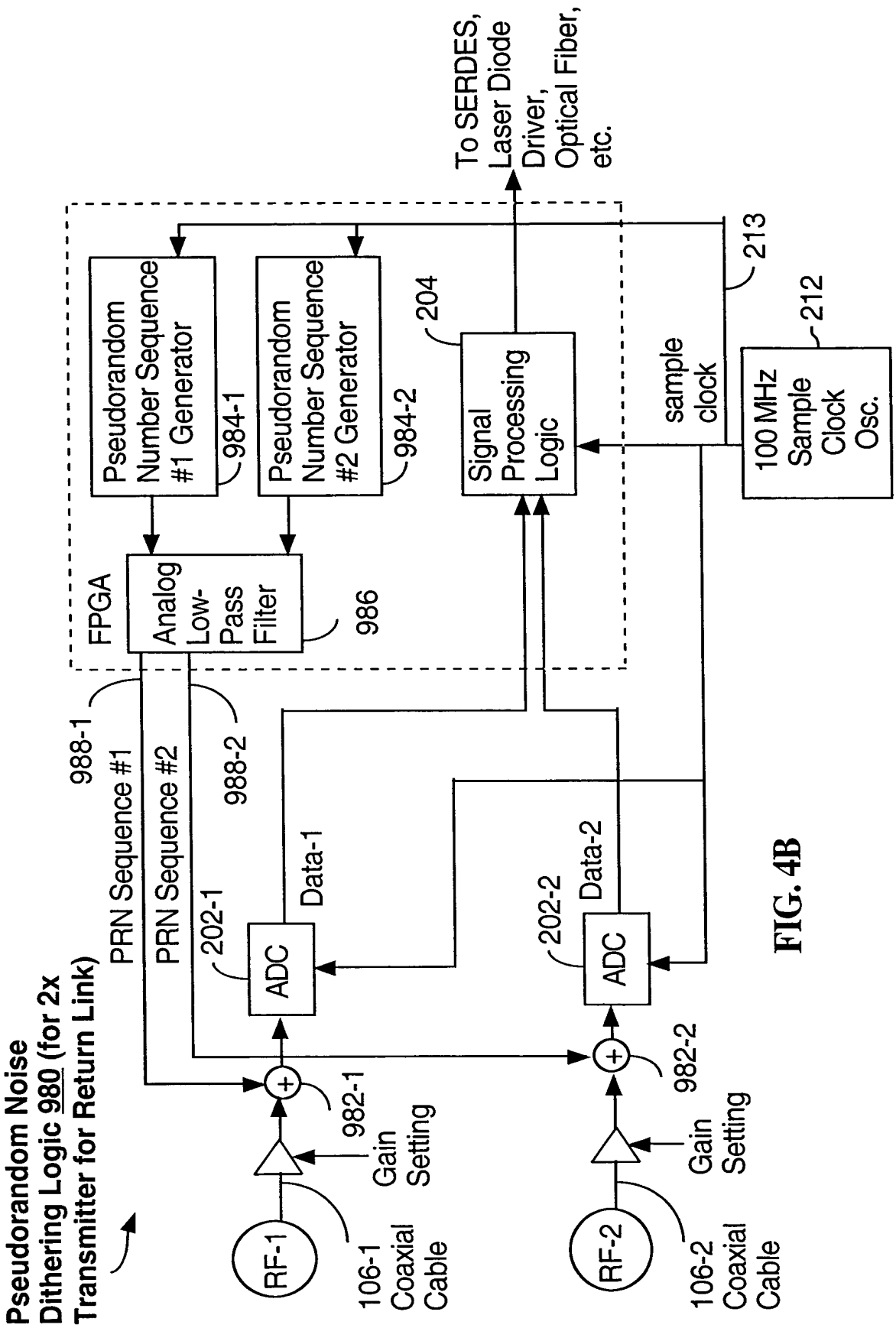

Pseudorandom Noise
Dithering Logic 980 (for 2x
Transmitter for Return Link)
RF-1
106-1
Coaxial
Cable
Gain
Setting
982-1
RF-2
106-2
Coaxial
Cable
Gain
Setting
982-2
ADC
202-1
Data-1
ADC
202-2
Data-2
PRN Sequence #1
PRN Sequence #2
988-1
988-2
FPGA
Analog
Low-
Pass
Filter
986
Pseudorandom
Number Sequence
#1 Generator
984-1
Pseudorandom
Number Sequence
#2 Generator
984-2
204
Signal
Processing
Logic
sample
clock
213
100 MHz
Sample
Clock
Osc.
212
To SERDES,
Laser Diode
Driver,
Optical Fiber,
etc.

FIG. 4B

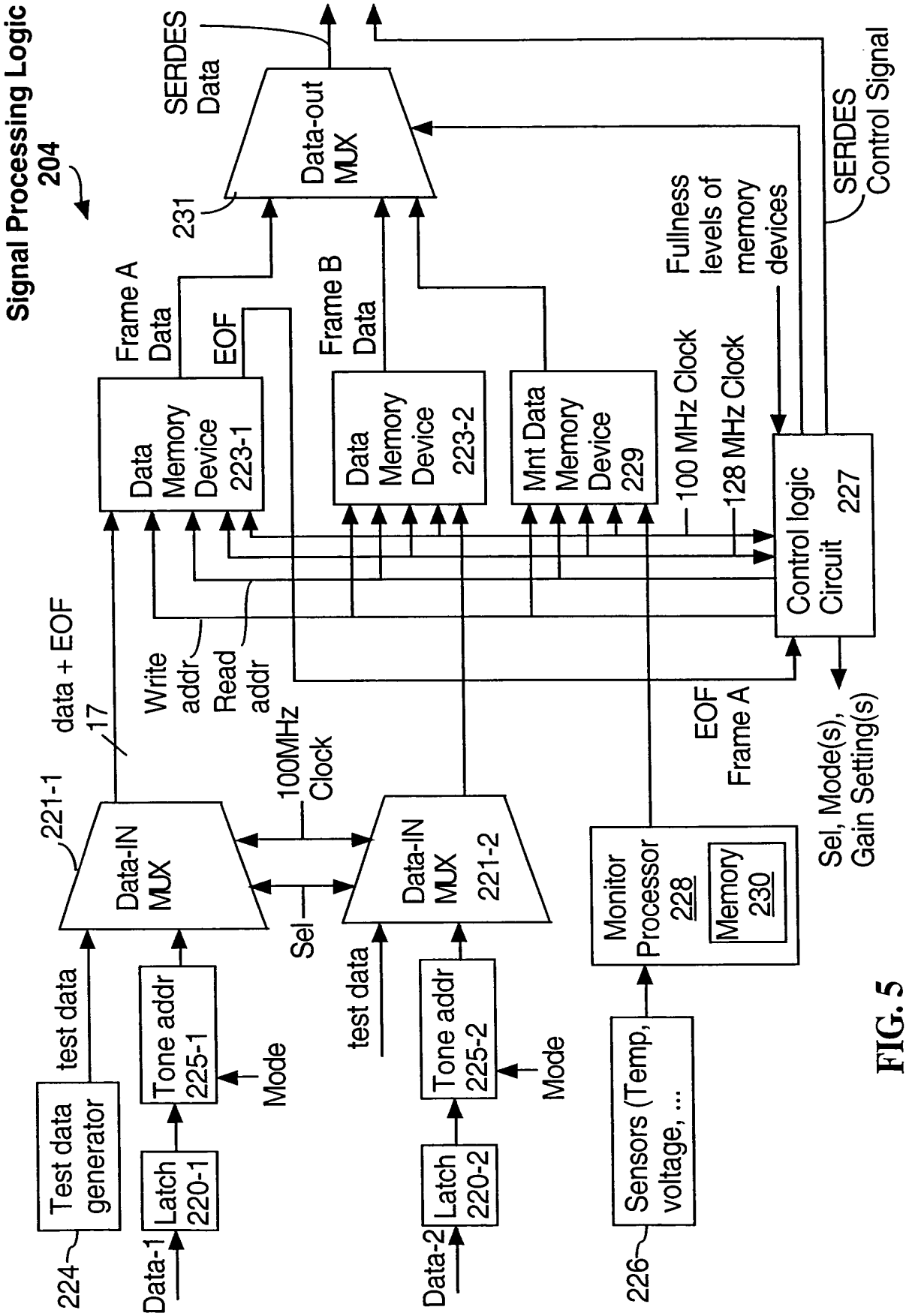

Signal Processing Logic
204
SERDES
Data
Data-out
MUX
231
SERDES
Control Signal
Frame A
Data
EOF
Frame B
Data
Fullness
levels of
memory
devices
Data
Memory
Device
223-1
Data
Memory
Device
223-2
Mnt Data
Memory
Device
229
100 MHz Clock
128 MHz Clock
Control logic
Circuit
227
data + EOF
17
Write
addr
Read
addr
100MHz
Clock
EOF
Frame A
221-1
Data-IN
MUX
Data-IN
MUX
221-2
Sel
Sel, Mode(s),
Gain Setting(s)
Monitor
Processor
228
Memory
230
test data
Tone addr
225-1
Mode
test data
Tone addr
225-2
Mode
Test data
generator
Latch
220-1
Latch
220-2
Sensors (Temp,
voltage, ...
224
Data-1
Data-2
226

FIG. 5

FIG. 6A

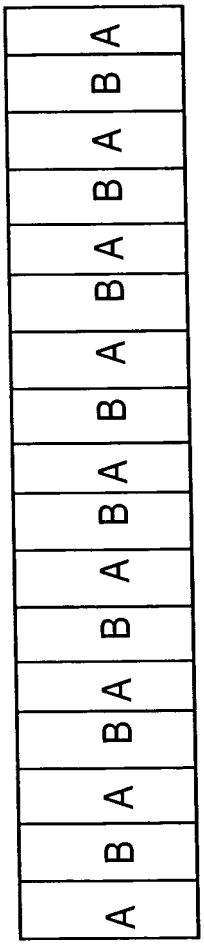


FIG. 6B

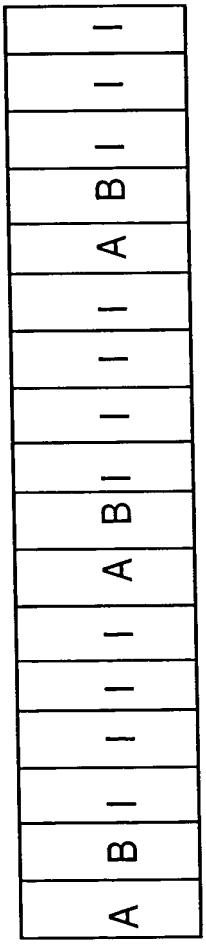
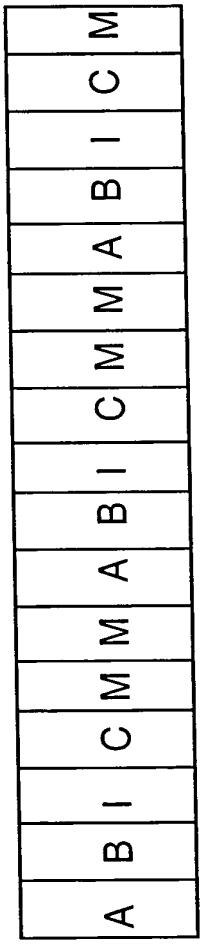


FIG. 6C



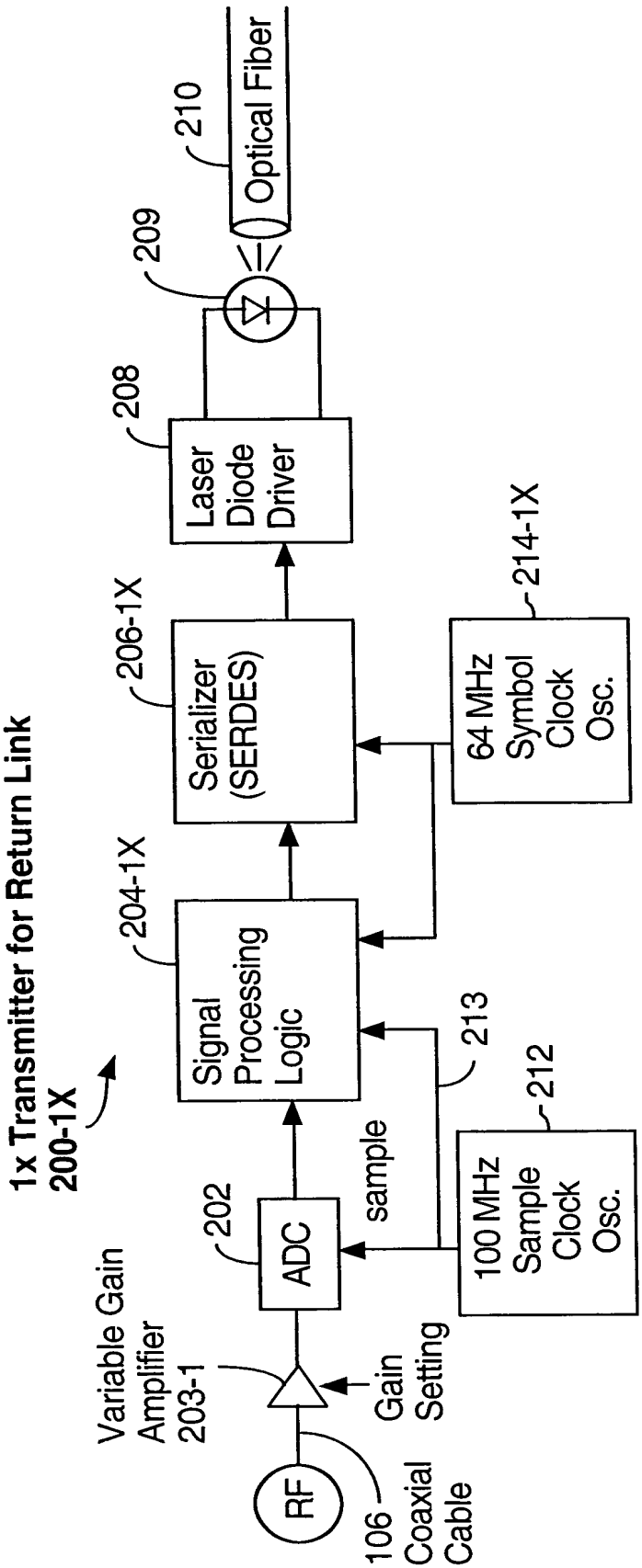

1x Transmitter for Return Link
200-1X
RF
106
Coaxial Cable
Variable Gain Amplifier
203-1
Gain Setting
202
ADC
sample
204-1X
Signal Processing Logic
213
212
100 MHz Sample Clock Osc.
206-1X
Serializer (SERDES)
214-1X
64 MHz Symbol Clock Osc.
208
Laser Diode Driver
209
210
Optical Fiber

FIG. 7

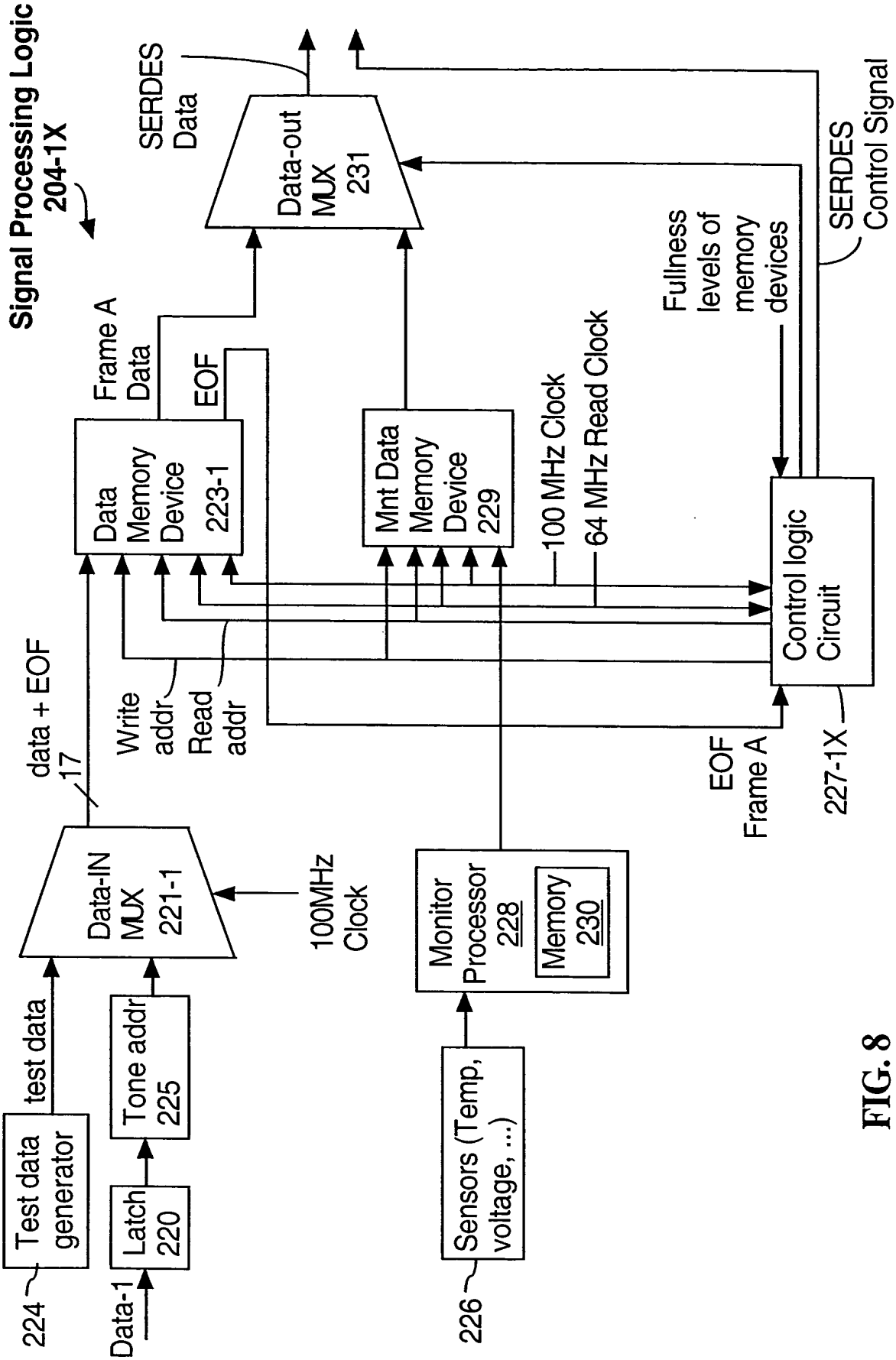

Signal Processing Logic
204-1X
SERDES
Data
Data-out
MUX
231
SERDES
Control Signal
Frame A
Data
EOF
Data
Memory
Device
223-1
Mnt Data
Memory
Device
229
100 MHz Clock
64 MHz Read Clock
Fullness
levels of
memory
devices
Control logic
Circuit
data + EOF
17
Write
addr
Read
addr
EOF
Frame A
227-1X
Data-IN
MUX
221-1
100MHz
Clock
Monitor
Processor
228
Memory
230
test data
Test data
generator
Tone addr
225
Latch
220
Sensors (Temp,
voltage, ...)
224
Data-1
226

FIG. 8

Title: RETURN PATH TRANSMITTER WITH EXTENDED DIGITAL PROCESSING CIRCUITRY
Inventors: Andrew R. Williams
Docket No.: 15436.253.78.1

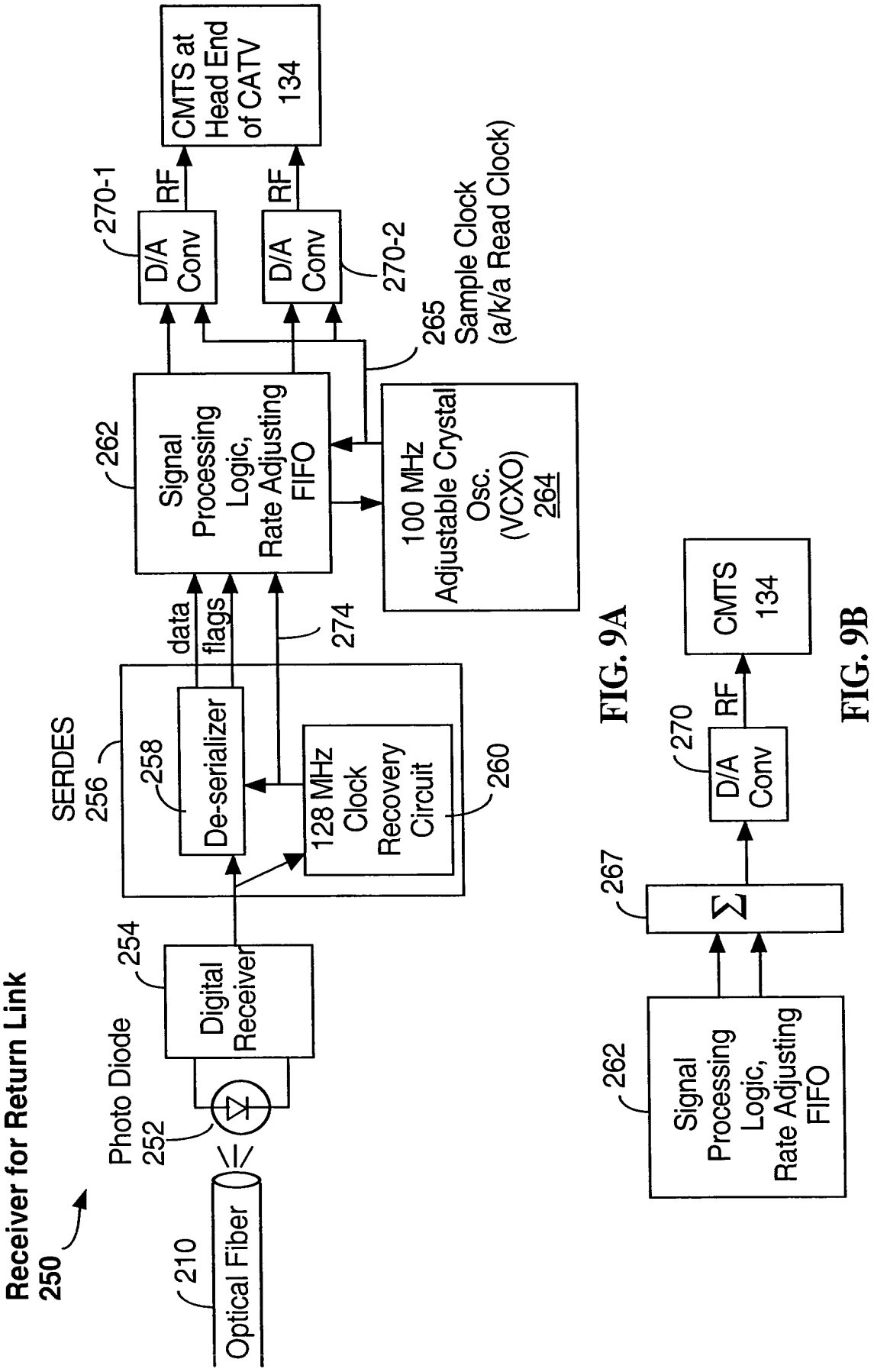


FIG. 9A

FIG. 9B

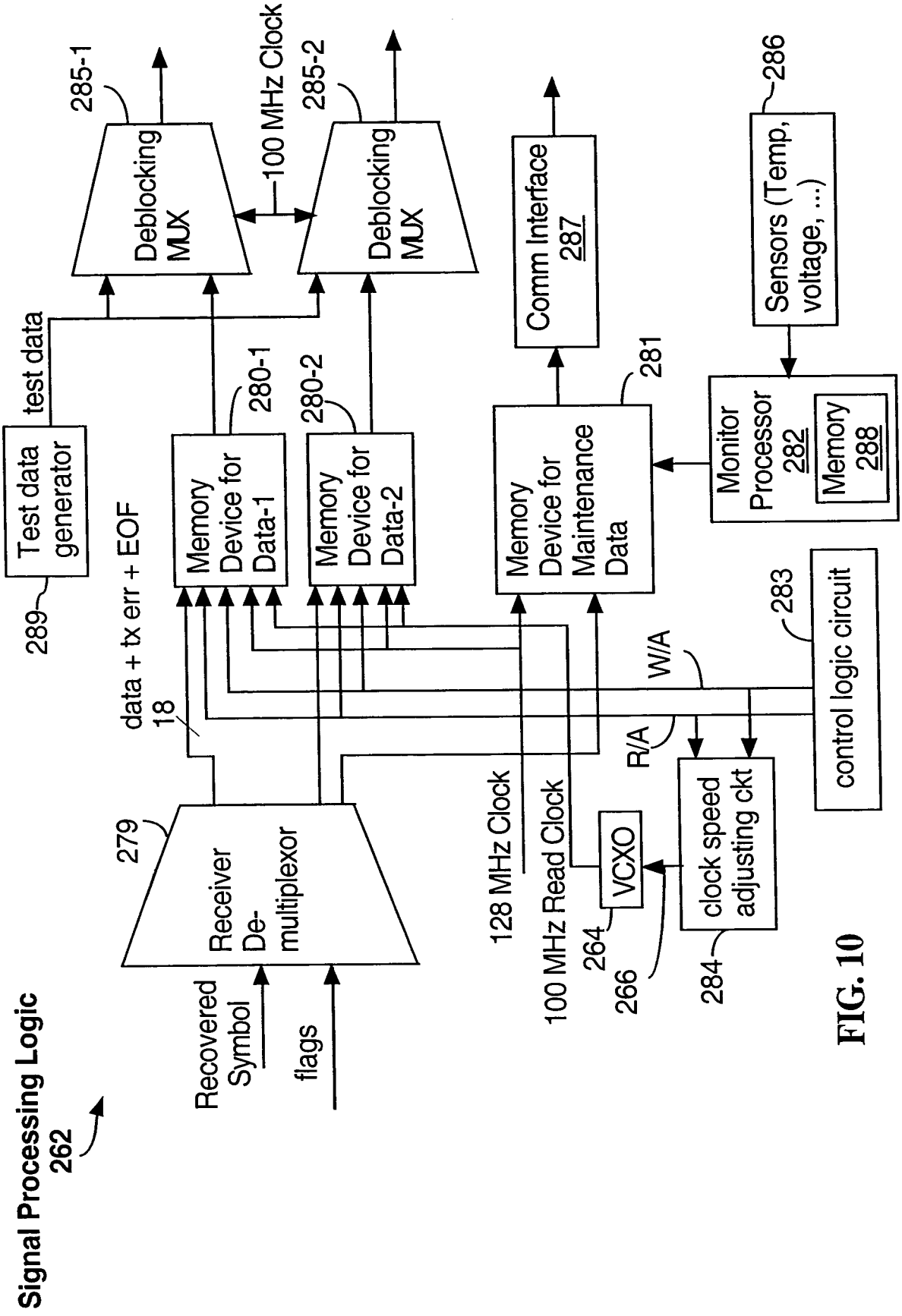
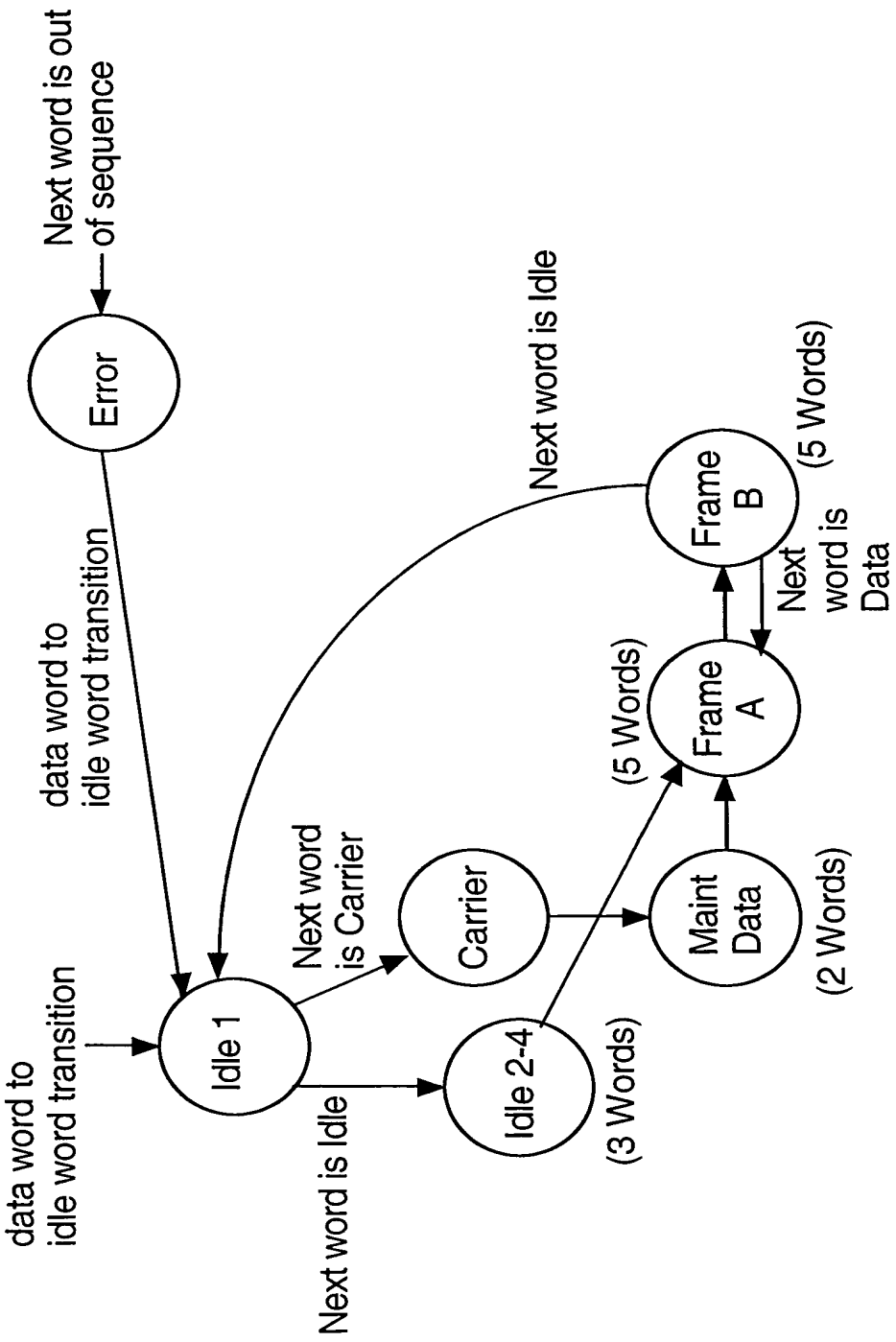

Signal Processing Logic
262
285-1
Deblocking MUX
100 MHz Clock
285-2
Deblocking MUX
Comm Interface
287
286
Sensors (Temp, voltage, ...)
test data
Test data generator
289
280-1
Memory Device for Data-1
280-2
Memory Device for Data-2
281
Memory Device for Maintenance Data
Monitor Processor
282
Memory
288
data + tx err + EOF
18
W/A
R/A
283
control logic circuit
279
Receiver De-multiplexor
128 MHz Clock
100 MHz Read Clock
VCXO
264
266
clock speed adjusting ckt
284
Recovered Symbol
flags

FIG. 10



State Diagram for Dual Channel Receiver Demultiplexor

FIG. 11

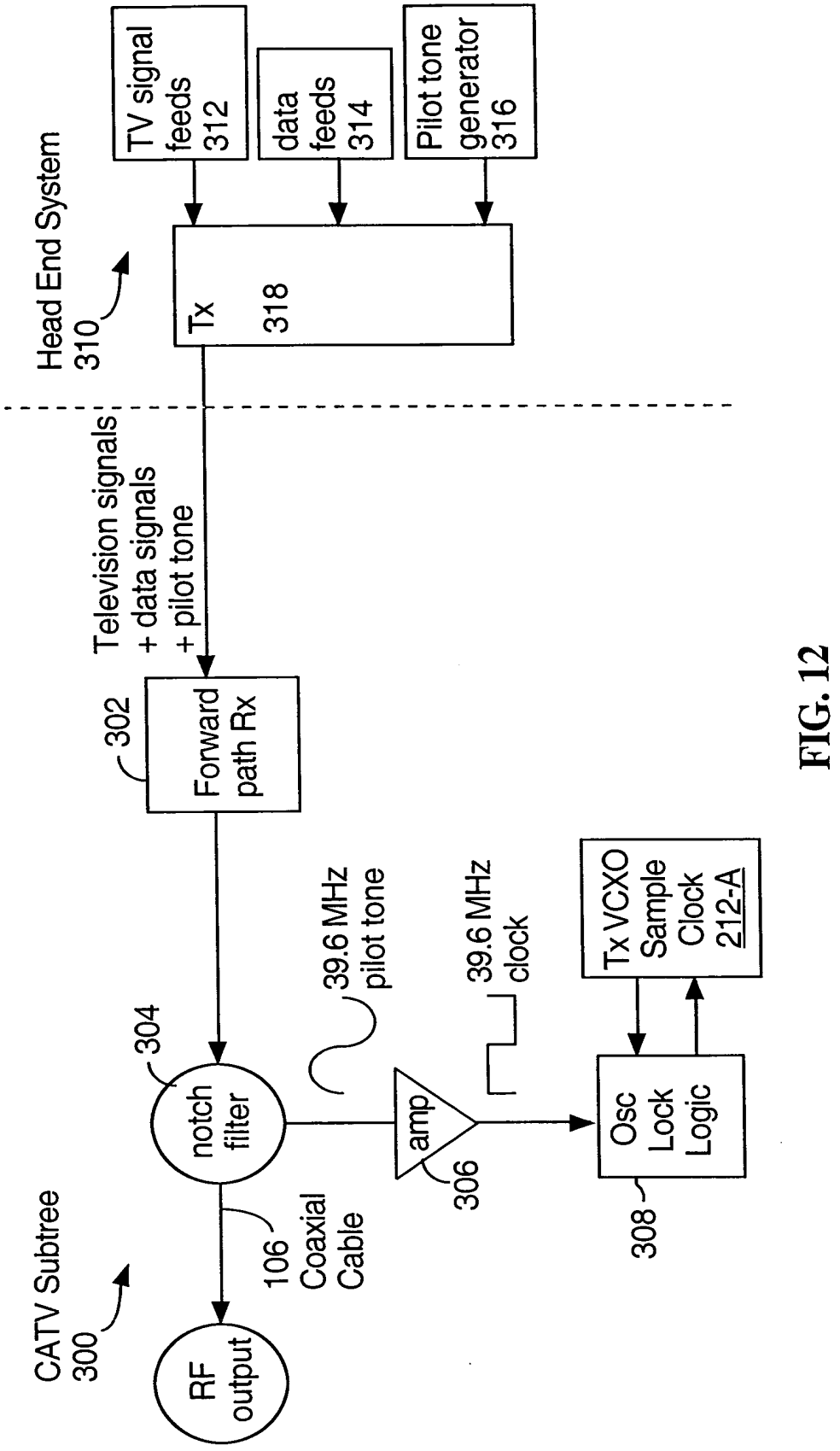

Head End System
310
TV signal feeds 312
data feeds 314
Pilot tone generator 316
Tx 318
Television signals + data signals + pilot tone
302
Forward path Rx
304
notch filter
39.6 MHz pilot tone
39.6 MHz clock
amp
306
Tx VCXO Sample Clock 212-A
Osc Lock Logic
308
CATV Subtree
300
106 Coaxial Cable
RF output

FIG. 12

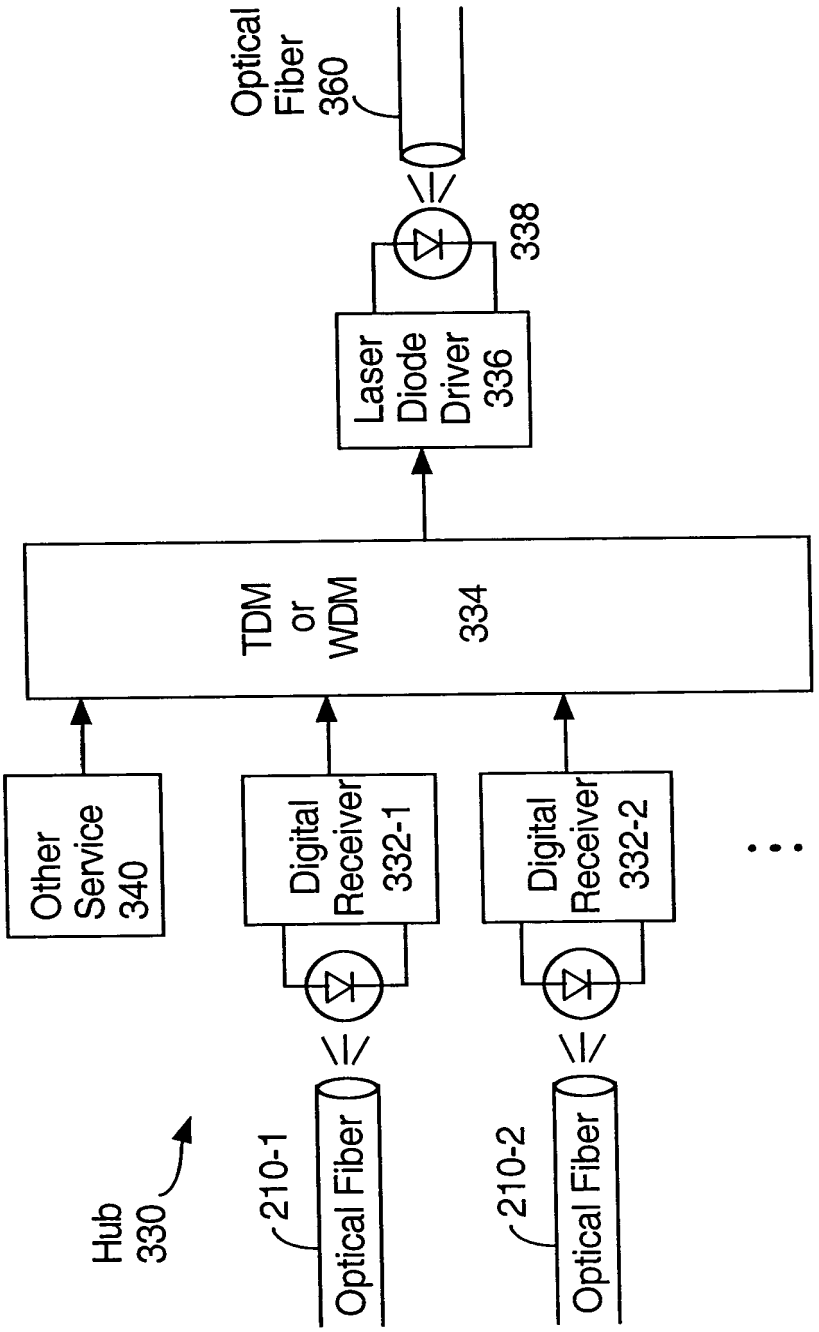

Optical Fiber 360
338
Laser Diode Driver 336
TDM or WDM 334
Other Service 340
Digital Receiver 332-1
Digital Receiver 332-2
Hub 330
210-1 Optical Fiber
210-2 Optical Fiber

FIG. 13

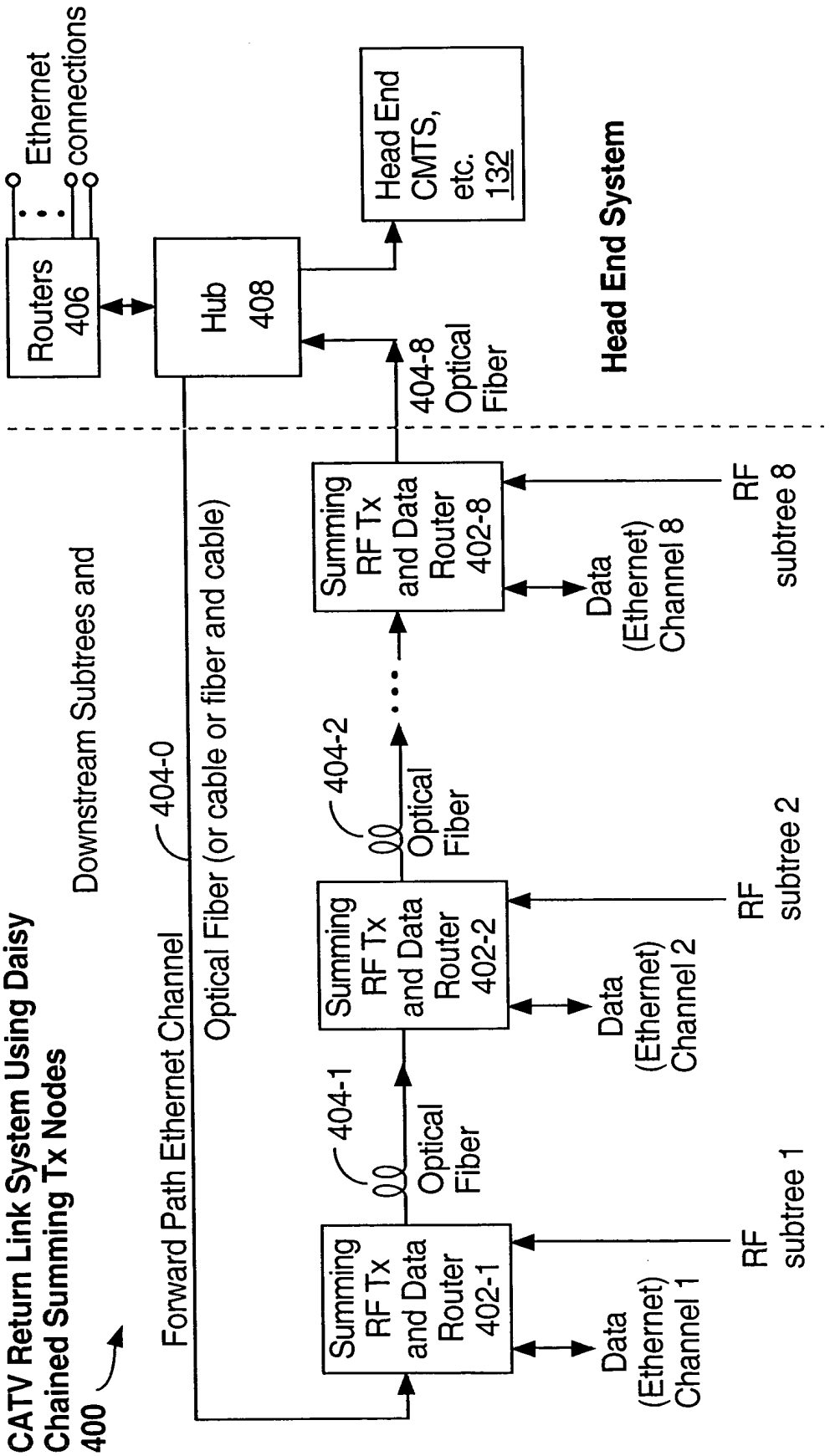

CATV Return Link System Using Daisy Chained Summing Tx Nodes
400
Downstream Subtrees and
Forward Path Ethernet Channel
Optical Fiber (or cable or fiber and cable)
404-0
Routers 406
Ethernet connections
Hub 408
Head End CMTS, etc. 132
Head End System
404-8 Optical Fiber
Summing RF Tx and Data Router 402-8
Data (Ethernet) Channel 8
RF subtree 8
404-2
Optical Fiber
Summing RF Tx and Data Router 402-2
Data (Ethernet) Channel 2
RF subtree 2
404-1
Optical Fiber
Summing RF Tx and Data Router 402-1
Data (Ethernet) Channel 1
RF subtree 1

FIG. 14

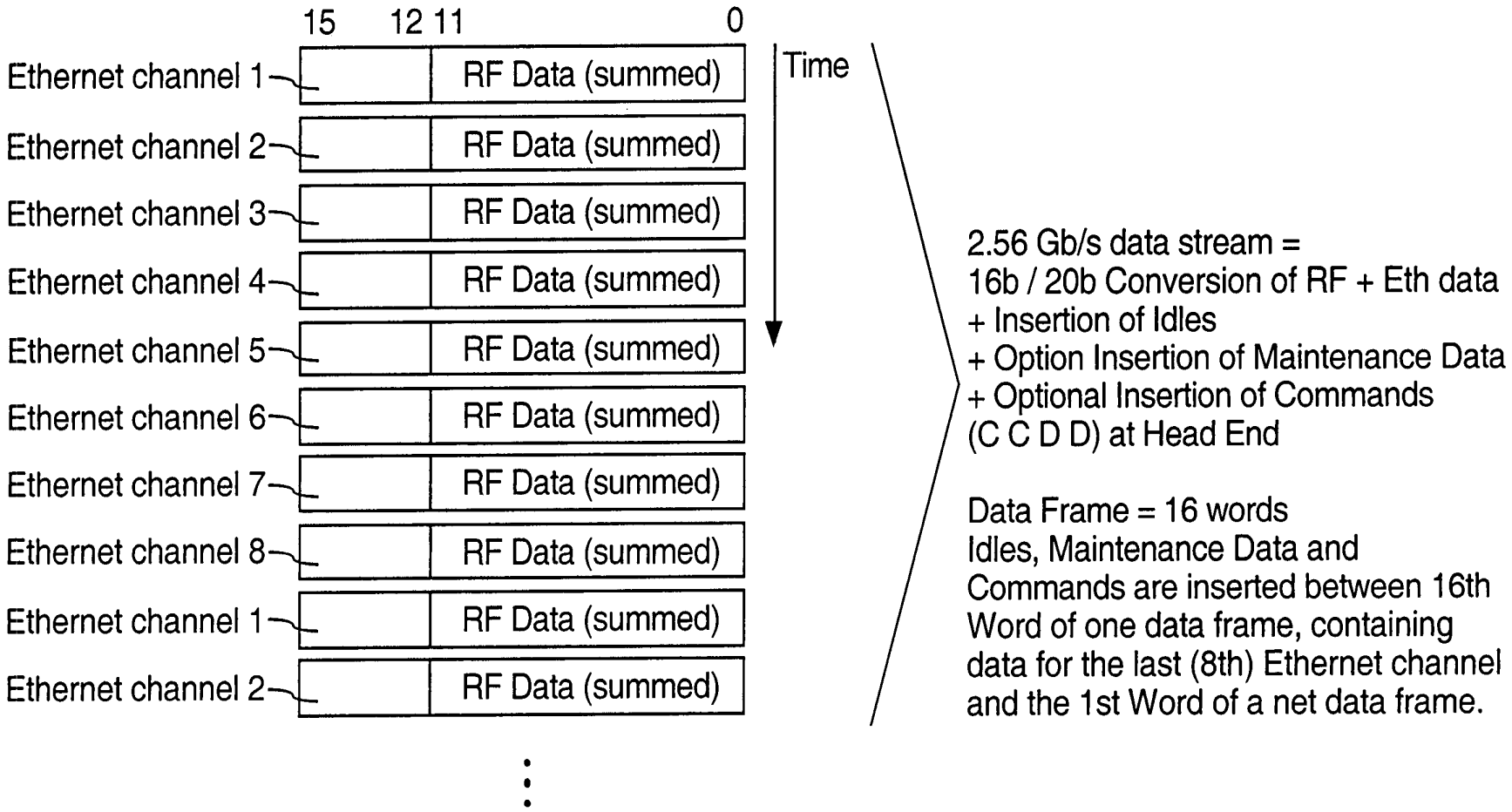

15
12 11
0
Time
Ethernet channel 1
Ethernet channel 2
Ethernet channel 3
Ethernet channel 4
Ethernet channel 5
Ethernet channel 6
Ethernet channel 7
Ethernet channel 8
Ethernet channel 1
Ethernet channel 2
RF Data (summed)
2.56 Gb/s data stream =
16b / 20b Conversion of RF + Eth data
+ Insertion of Idles
+ Option Insertion of Maintenance Data
+ Optional Insertion of Commands
(C C D D) at Head End
Data Frame = 16 words
Idles, Maintenance Data and
Commands are inserted between 16th
Word of one data frame, containing
data for the last (8th) Ethernet channel
and the 1st Word of a net data frame.

FIG. 15

Title: RETURN PATH TRANSMITTER WITH EXTENDED DIGITAL PROCESSING CIRCUITRY
Inventors: Andrew R. Williams
Docket No.: 15436.253.78.1

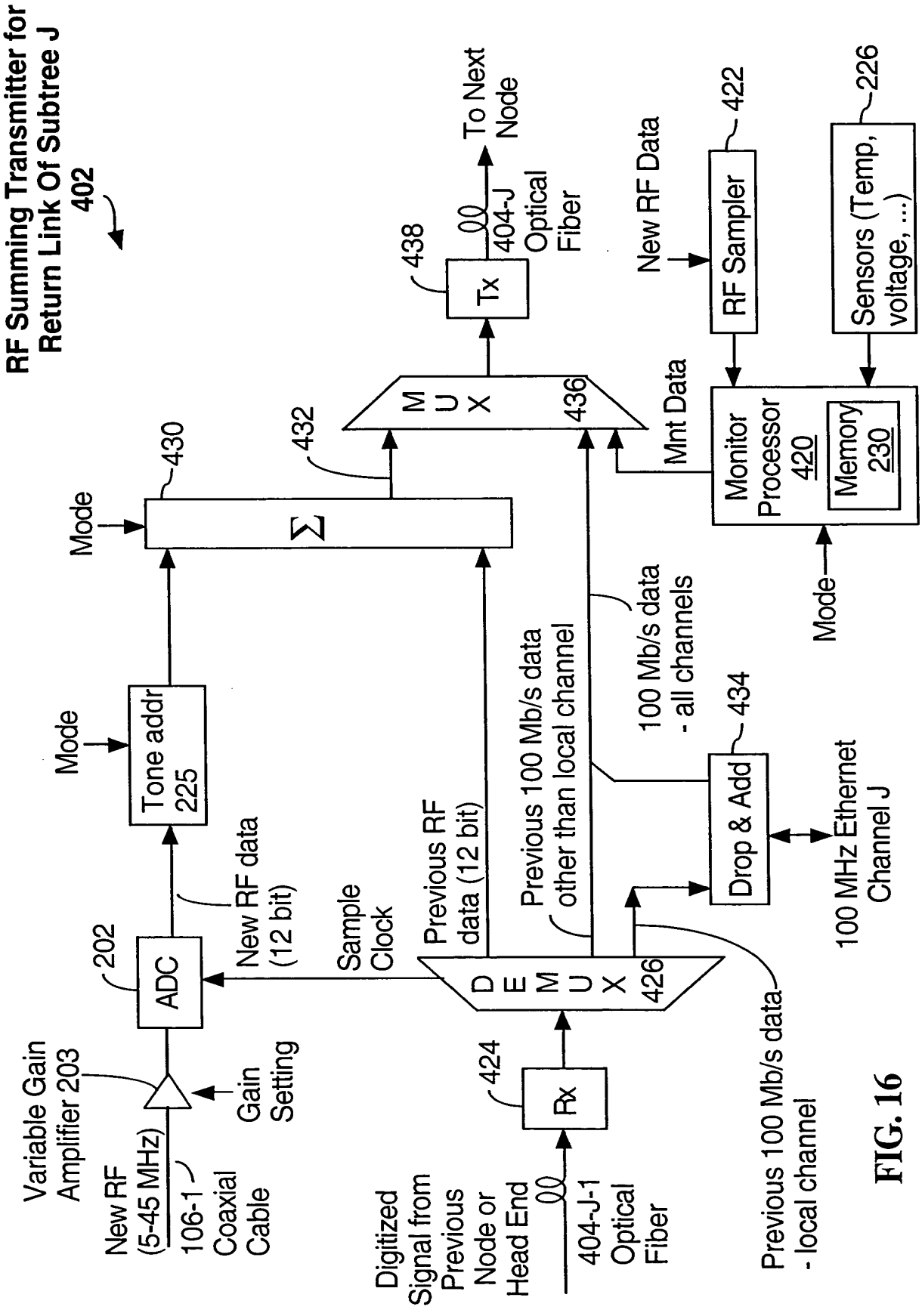

RF Summing Transmitter for Return Link Of Subtree J
402
Variable Gain Amplifier 203
New RF (5-45 MHz)
106-1 Coaxial Cable
Gain Setting
ADC
202
New RF data (12 bit)
Sample Clock
Tone addr 225
Mode
Mode
430
Σ
432
MUX
436
Tx
438
404-J Optical Fiber
To Next Node
DEMUX
426
Previous RF data (12 bit)
Previous 100 Mb/s data other than local channel
100 Mb/s data - all channels
Rx
424
Digitized Signal from Previous Node or Head End
404-J-1 Optical Fiber
Drop & Add
434
100 MHz Ethernet Channel J
Previous 100 Mb/s data - local channel
New RF Data
RF Sampler
422
Sensors (Temp, voltage, ...)
226
Mnt Data
Monitor Processor 420
Memory 230
Mode

FIG. 16

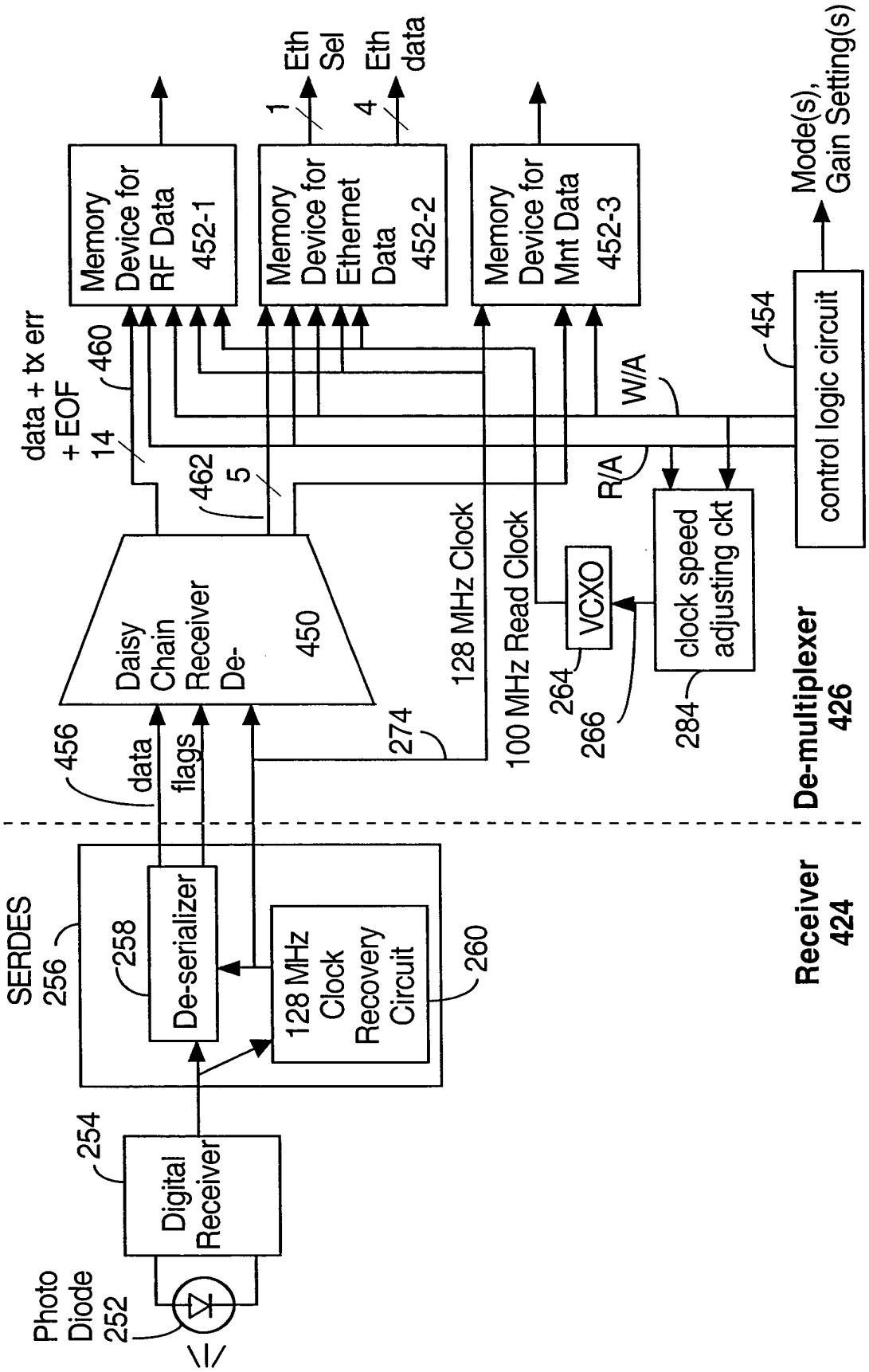


Photo Diode 252
Digital Receiver
254
SERDES 256
De-serializer
258
128 MHz Clock Recovery Circuit
260
Receiver 424
De-multiplexer 426
data
flags
456
Daisy Chain Receiver De-
450
128 MHz Clock
274
100 MHz Read Clock
VCXO
264
266
clock speed adjusting ckt
284
R/A
W/A
control logic circuit
454
Mode(s), Gain Setting(s)
data + tx err + EOF
14
460
462
5
Memory Device for RF Data 452-1
Memory Device for Ethernet Data 452-2
Memory Device for Mnt Data 452-3
1
Eth Sel
4
Eth data

FIG. 17

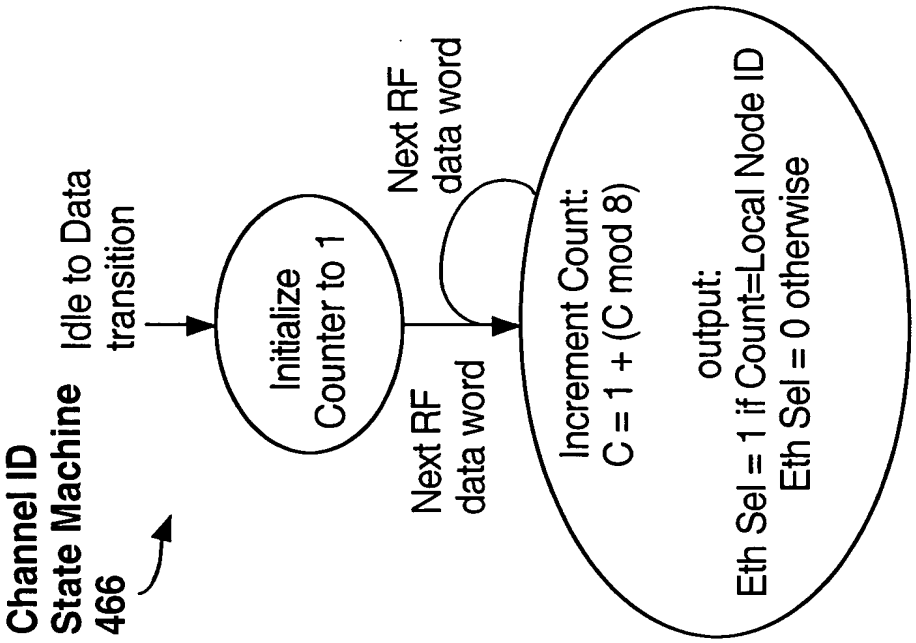

Channel ID
State Machine
466
Idle to Data
transition
Initialize
Counter to 1
Next RF
data word
Next RF
data word
Increment Count:
C = 1 + (C mod 8)
output:
Eth Sel = 1 if Count=Local Node ID
Eth Sel = 0 otherwise

FIG. 19

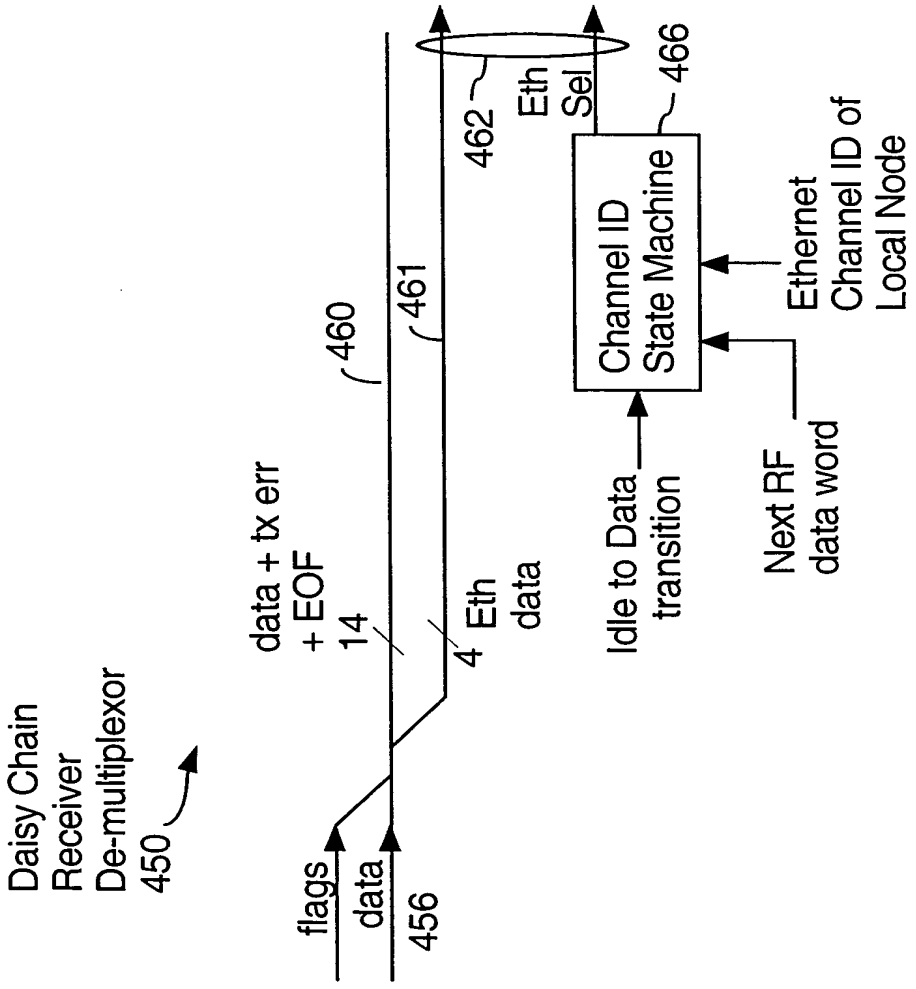

Daisy Chain
Receiver
De-multiplexor
450
flags
data
456
data + tx err
+ EOF
14
4 Eth
data
460
461
462
Eth
Sel
466
Channel ID
State Machine
Idle to Data
transition
Next RF
data word
Ethernet
Channel ID of
Local Node

FIG. 18

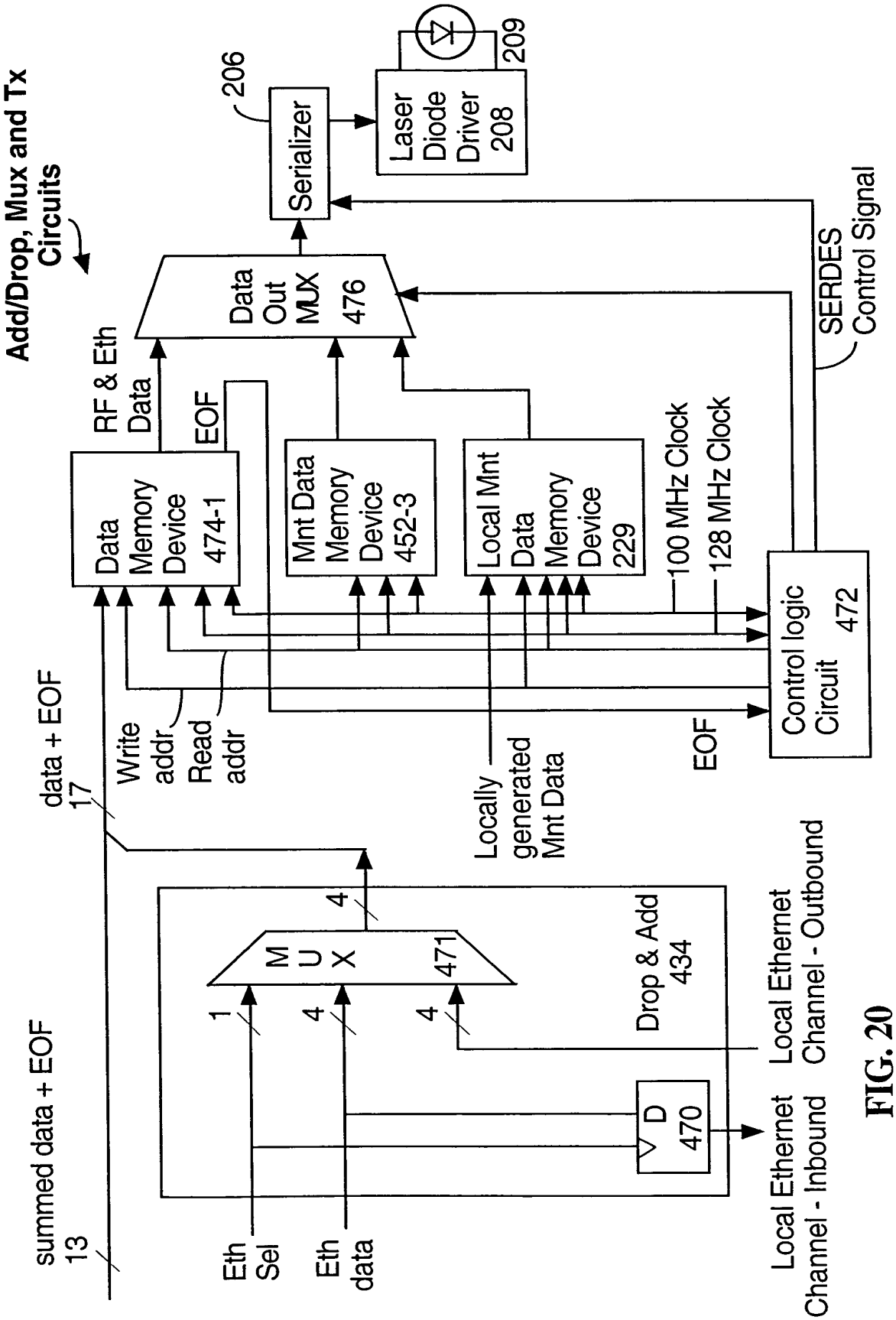

Add/Drop, Mux and Tx Circuits
206
Serializer
Laser Diode Driver 208
209
Data Out MUX 476
SERDES Control Signal
RF & Eth Data
EOF
Data Memory Device 474-1
Mnt Data Memory Device 452-3
Local Mnt Data Memory Device 229
100 MHz Clock
128 MHz Clock
Control logic Circuit 472
data + EOF 17
Write addr
Read addr
Locally generated Mnt Data
EOF
summed data + EOF 13
M U X
4
471
1
4
4
Drop & Add 434
D 470
Eth Sel
Eth data
Local Ethernet Channel - Inbound
Local Ethernet Channel - Outbound

FIG. 20

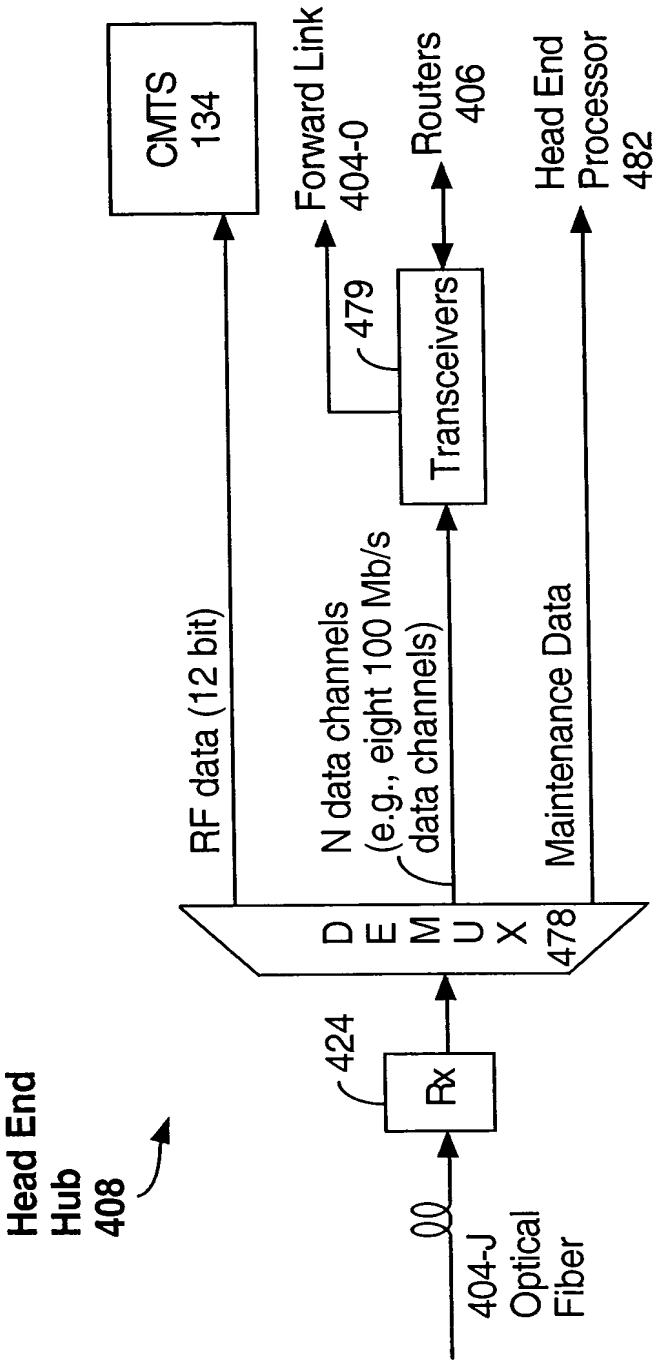

Head End
Hub
408
404-J
Optical
Fiber
424
Rx
DEMUX
478
RF data (12 bit)
N data channels
(e.g., eight 100 Mb/s
data channels)
Maintenance Data
479
Transceivers
Forward Link
404-0
Routers
406
Head End
Processor
482
CMTS
134

FIG. 21

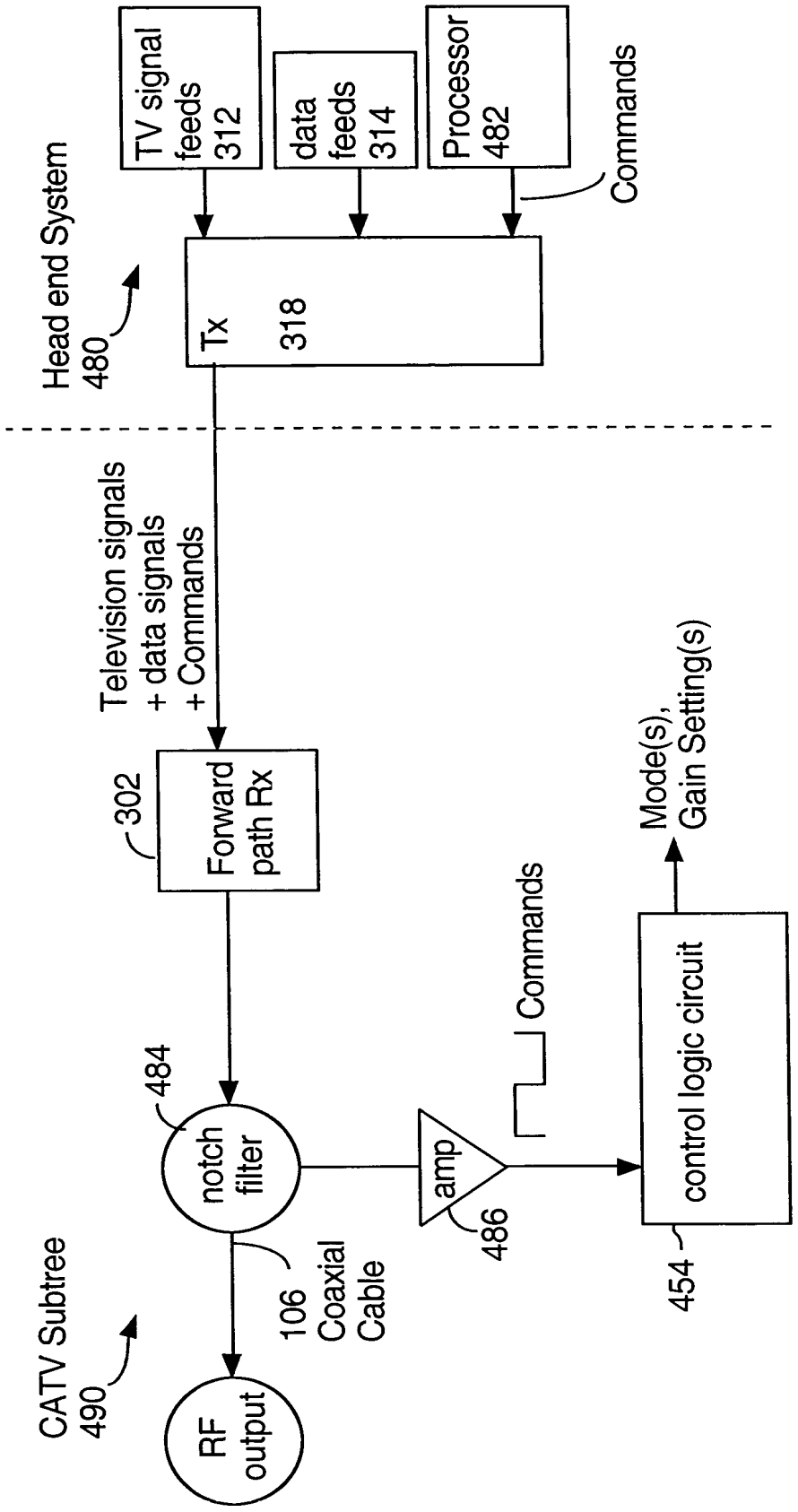

TV signal feeds 312
data feeds 314
Processor 482
Commands
Head end System 480
Tx 318
Television signals + data signals + Commands
302
Forward path Rx
484
notch filter
amp
486
Commands
Mode(s), Gain Setting(s)
control logic circuit
454
106 Coaxial Cable
CATV Subtree 490
RF output

FIG. 22

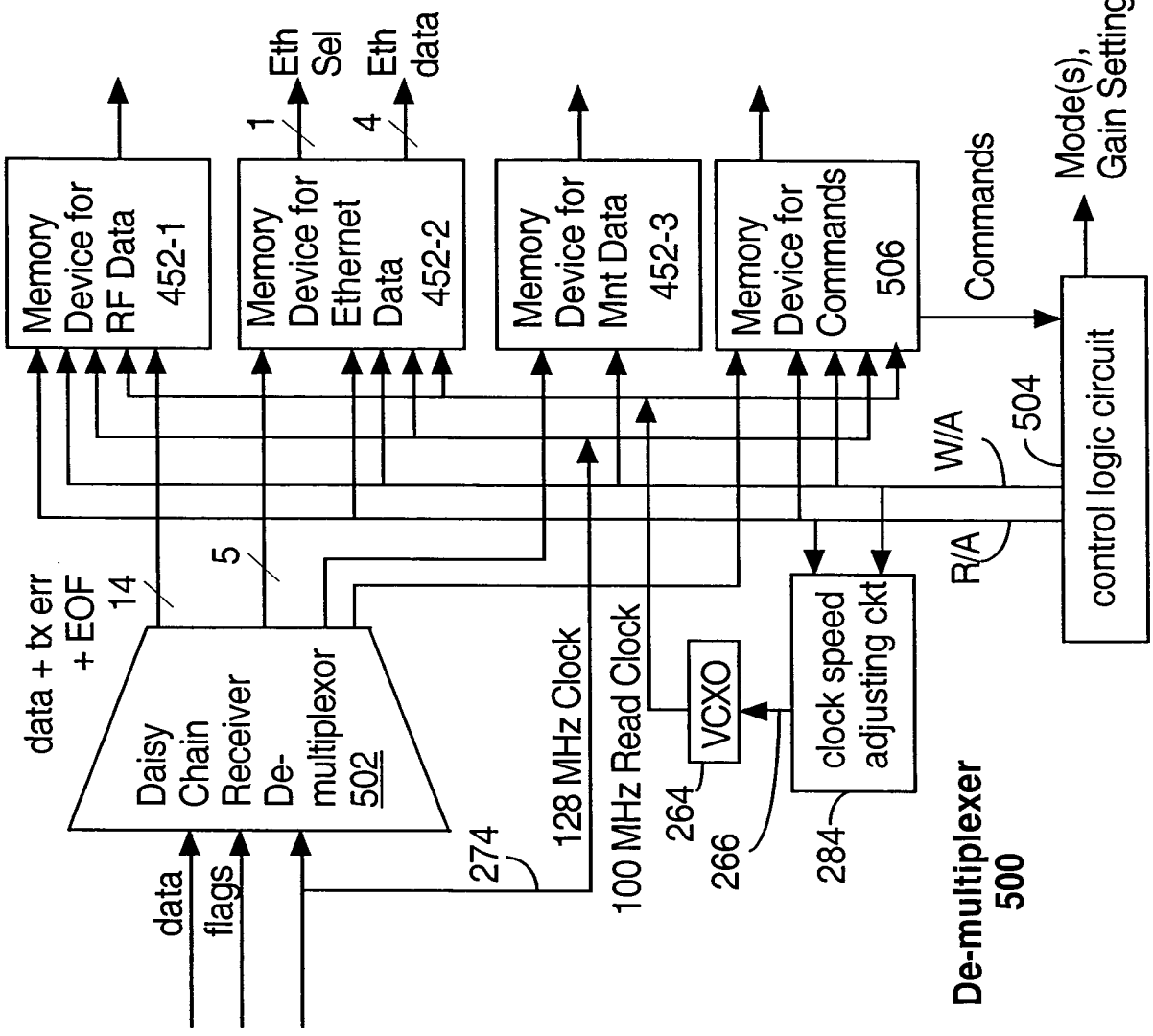

Memory Device for RF Data 452-1
Memory Device for Ethernet Data 452-2
Memory Device for Mnt Data 452-3
Memory Device for Commands 506
1
Eth Sel
4
Eth data
Commands
Mode(s), Gain Setting(s)
control logic circuit
W/A
504
R/A
data + tx err + EOF
14
5
Daisy Chain Receiver De-multiplexor 502
data
flags
274
128 MHz Clock
100 MHz Read Clock
VCXO
264
266
clock speed adjusting ckt
284
De-multiplexer 500

FIG. 23

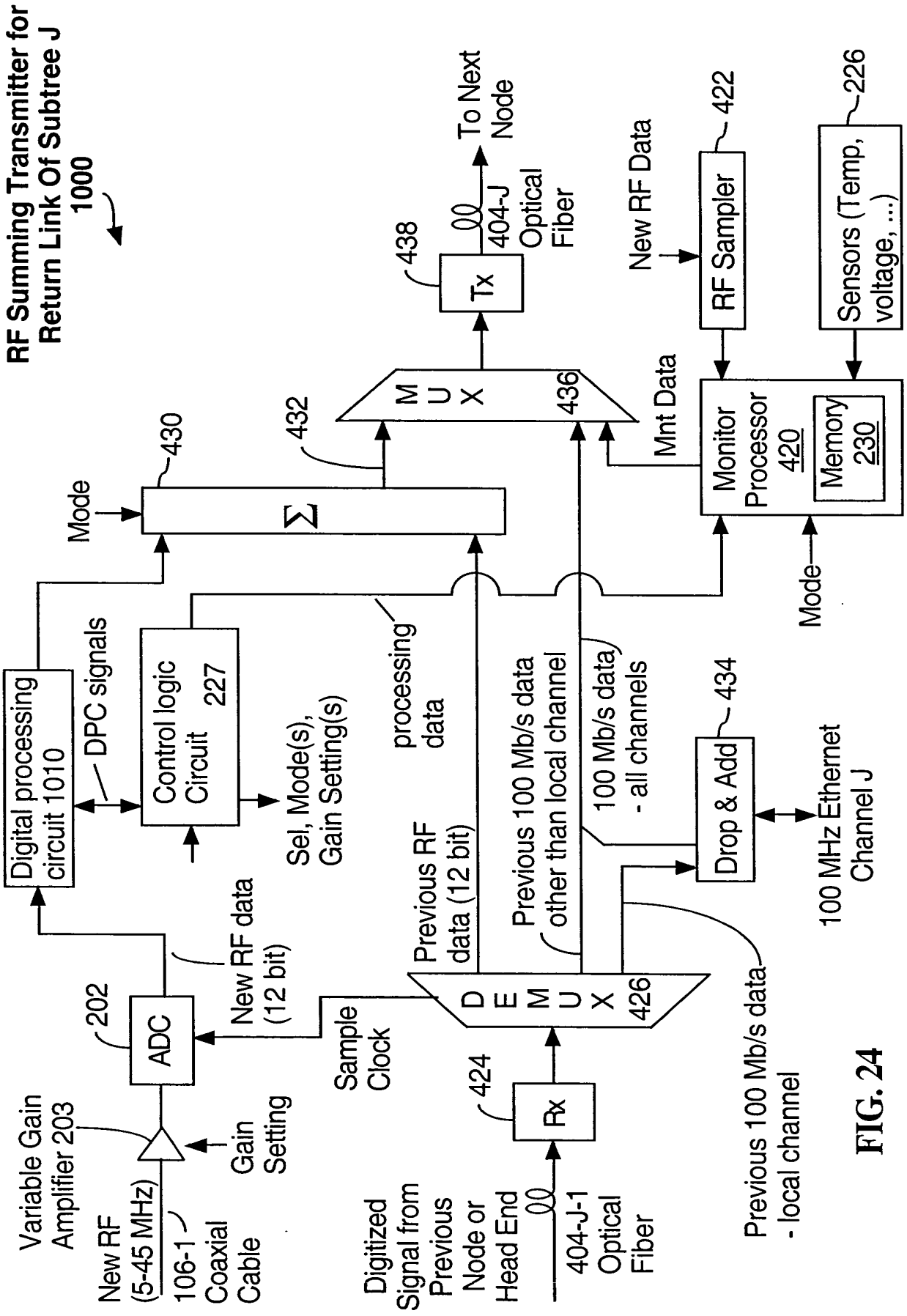

RF Summing Transmitter for Return Link Of Subtree J
1000
To Next Node
438
Tx
404-J Optical Fiber
New RF Data
422
RF Sampler
226
Sensors (Temp, voltage, ...)
Mode
430
Σ
432
M U X
436
Mnt Data
Monitor Processor 420
Memory 230
Mode
Digital processing circuit 1010
DPC signals
Control logic Circuit 227
Sel, Mode(s), Gain Setting(s)
processing data
Previous RF data (12 bit)
Previous 100 Mb/s data other than local channel
100 Mb/s data - all channels
Drop & Add
434
100 MHz Ethernet Channel J
202
ADC
New RF data (12 bit)
Sample Clock
D E M U X
426
424
Rx
Variable Gain Amplifier 203
Gain Setting
New RF (5-45 MHz)
106-1 Coaxial Cable
Digitized Signal from Previous Node or Head End
404-J-1 Optical Fiber
Previous 100 Mb/s data - local channel

FIG. 24

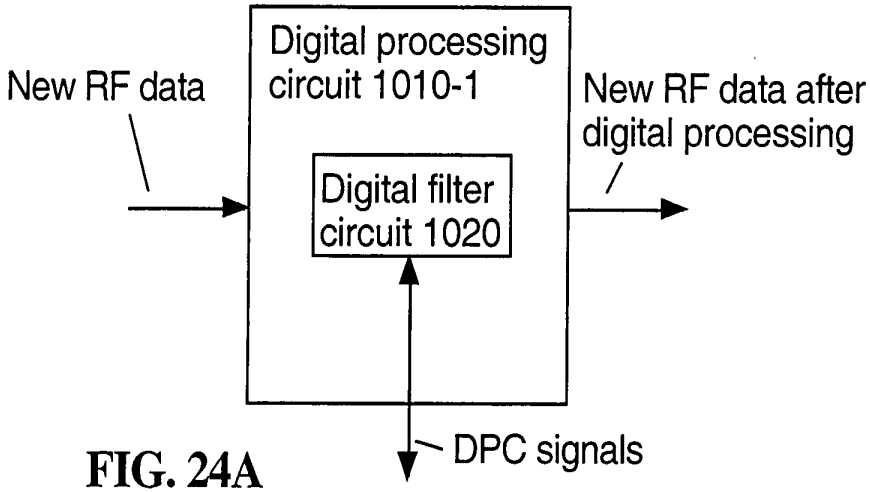


FIG. 24A

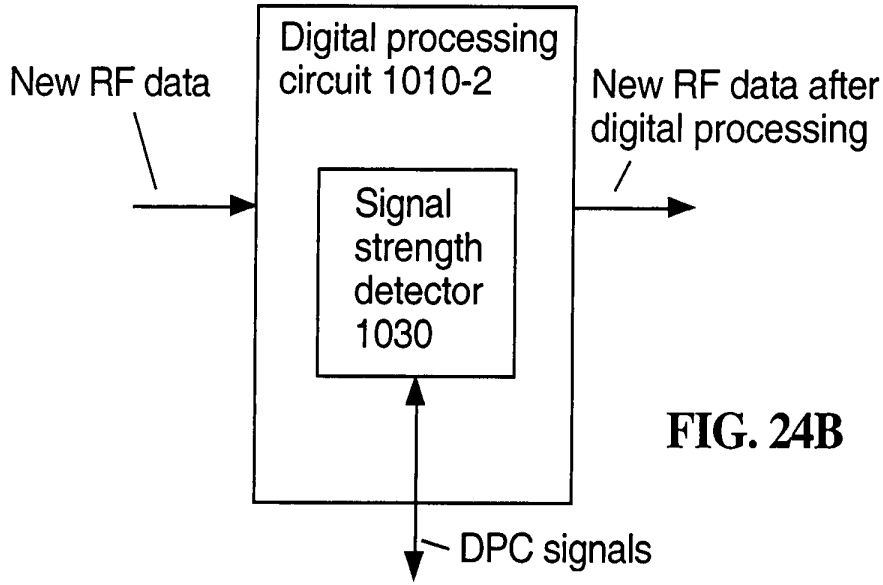


FIG. 24B

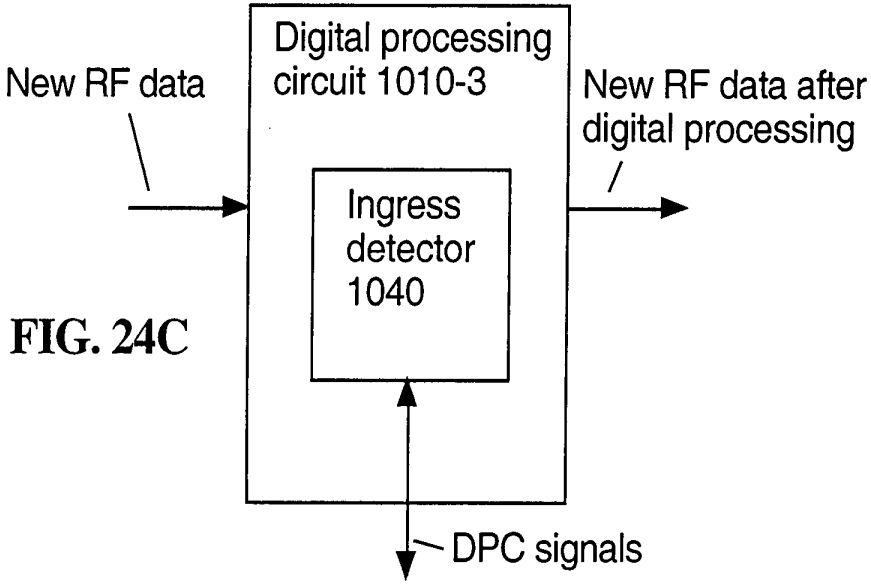


FIG. 24C

Title: RETURN PATH TRANSMITTER WITH EXTENDED DIGITAL PROCESSING CIRCUITRY
Inventors: Andrew R. Williams
Docket No.: 15436.253.78.1